Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Previously Presented) The method of Claim 6, wherein the step of shifting truncates a selected number of least significant bits of the intermediate result.

3. (Original) The method of Claim 2, wherein the step of rounding adds a rounding value to the combined product to form the intermediate result, and wherein the step of shifting shifts the intermediate result right by a selected shift amount.

4. (Original) The method of Claim 3, wherein the rounding value is 2**n and the selected shift amount is n+1.

5. (Original) The method of Claim 4, wherein n has a fixed value of fourteen.

6. (Previously Presented) A method of performing a product operation with rounding in a microprocessor in response to a single rounding multiplication instruction, the method comprising the steps of:

fetching a first pair of elements and a second pair of elements;

forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements, wherein the first element of the first pair of elements is a most significant element of the first pair of elements;

combining the most significant product with the least significant product to form a combined product, wherein combining comprises shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product;

rounding the combined product to form an intermediate result; and

shifting the intermediate result a selected amount to form a final result.

7. (Canceled)

8. (Withdrawn) A method of performing a product operation with rounding in a microprocessor in response to a single rounding multiplication instruction, the method comprising the steps of:

fetching a first pair of elements and a second pair of elements;

forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements;

rounding the least significant product to form a rounded least significant product;

shifting the rounded least significant result a selected amount to form a truncated least significant result; and

combining the most significant product with the truncated least significant product to form a final result.

9. (Currently Amended) A digital system having a microprocessor operable to execute a rounding multiplication instruction, wherein the microprocessor comprises:

storage circuitry for holding pairs of elements;

a multiply circuit connected to receive a ~~first~~ number of the pairs of elements from the storage circuitry ~~in a first execution phase of the microprocessor~~ responsive to the multiplication instruction, the multiply circuit comprising a plurality of multipliers, wherein the plurality of multipliers form a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements, wherein the first element of the first pair of elements is a most significant element of the first pair of elements;

an arithmetic circuit connected to receive ~~a~~ the most significant product and ~~a~~ the least significant product from the plurality of multipliers, wherein the arithmetic circuit shifts the most significant product by a number of bits prior to adding the most significant product to the least significant product, the arithmetic circuit having a provision for mid-position rounding responsive to the rounding multiplication instruction; and

a shifter connected to receive an output of the arithmetic circuit, the shifter operable to shift a selected amount in response to the rounding multiplication instructions.

10. (Original) The digital system of Claim 9, wherein the arithmetic circuit has a additional input connected to a mid-position, wherein the additional input is asserted in response to the rounding multiplication instruction.

11. (Original) The digital system according to Claim 9 being a cellular telephone, further comprising:

an integrated keyboard connected to the processor via a keyboard adapter;

a display, connected to the processor via a display adapter;

radio frequency (RF) circuitry connected to the processor; and

an aerial connected to the RF circuitry.

12. (Previously Presented) A method of performing a product operation with rounding in a microprocessor in response to a single rounding multiplication instruction, the method comprising the steps of:

fetching a first pair of elements and a second pair of elements;

forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements, wherein the first element of the first pair of elements is a most significant element of the first pair of elements;

combining the most significant product with the least significant product to form a combined product;

rounding the combined product to form an intermediate result; and

shifting the intermediate result a selected amount to form a final result.

13. (Previously Presented) The method of Claim 12, wherein the step of shifting truncates a selected number of least significant bits of the intermediate result.

14. (Previously Presented) The method of Claim 13, wherein the step of rounding adds a rounding value to the combined product to form the intermediate result, and wherein the step of shifting shifts the intermediate result right by a selected shift amount.

15. (Previously Presented) The method of Claim 14, wherein the rounding value is 2**n and the selected shift amount is n+1.

16. (Previously Presented) The method of Claim 15, wherein n has a fixed value of fourteen.

17. (Currently Amended) A digital system having a microprocessor operable to execute a rounding multiplication instruction, wherein the microprocessor comprises:

storage circuitry for holding pairs of elements;

a multiply circuit connected to receive a ~~first~~ number of the pairs of elements from the storage circuitry ~~in a first execution phase of the microprocessor~~ responsive to the multiplication instruction, the multiply circuit comprising a plurality of multipliers, wherein the plurality of multipliers form a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements, wherein the first element of the first pair of elements is a most significant element of the first pair of elements;

an arithmetic circuit connected to receive a the most significant product and a the least significant product from the plurality of multipliers~~, the arithmetic circuit having a provision for mid-position rounding responsive to the rounding multiplication instruction~~; and

a shifter connected to receive an output of the arithmetic circuit~~, the shifter operable to shift a selected amount in response to the rounding multiplication instructions~~.

18. (Currently Amended) The digital system of Claim 17, wherein the arithmetic circuit has a provision for mid-position rounding responsive to the rounding multiplication instruction, wherein the arithmetic circuit has an additional input connected to a mid-position, wherein the additional input is asserted in response to the rounding multiplication instruction.

19. (Previously Presented) The digital system according to Claim 17 being a cellular telephone, further comprising:

an integrated keyboard connected to the processor via a keyboard adapter;

a display, connected to the processor via a display adapter;

radio frequency (RF) circuitry connected to the processor; and

an aerial connected to the RF circuitry.

20. (New) The digital system of claim 18, wherein the shifter is operable to shift a selected amount in response to the rounding multiplication instruction.